DAMASCENE METHOD CAPABLE OF AVOIDING COPPER EXTRUSION

DESCRIPTION

Background of Invention

[Para 1] 1. Field of the Invention

[Para 2] The present invention relates to a damascene method for fabricating a metal interconnect, and more particularly, to a damascene method capable of avoiding copper extrusion.

[Para 3] 2. Description of the Prior Art

[Para 4] In conventional integrated circuits, a metal interconnect is formed using aluminum and silicon dioxide. However, aluminum and silicon dioxide metal interconnects are not suitable for today's narrower line width and faster production speeds. Therefore, in recent years, the metal interconnect is formed with a damascene structure using copper and a dielectric material. The resistance of copper is approximately lower 40% than that of aluminum. The dielectric material can reduce the capacity effect of a metal conductive wire. Therefore, the damascene structure can decrease RC delay propagating when an electrical signal transmits and increase product performance.

[Para 5] A damascene method for fabricating the damascene structure mainly could be sub-classified into a method for fabricating a single damascene structure and a method for fabricating a dual damascene structure. Thereof, the method for fabricating a dual damascene is more complex, as shown in Fig.1. At least one copper conductive wire 14 is formed on a base layer 10 such as an interlayer dielectric. Although not shown, the copper conductive wire 14 could electrically connect to another conductive area below the base layer 10 through the conductive plug 12. A first dielectric layer 20 is

deposited on the copper conductive wire 14. A passivation 16 further would be formed between the conductive wire 14 and the first dielectric layer 20. A stop layer 22 is formed overlying the first dielectric layer 20. A second dielectric layer 24 is deposited on the stop layer 22. A hard mask 26 is formed on second dielectric layer 24. A dual damascene structure 30, exposing a portion of the copper conductive wire 14, is formed using the hard mask 26 to etch the first dielectric layer 20 and the second dielectric layer 24. A barrier layer 50 is deposited on the surface of the exposed copper conductive wire 14, the surface of the dual damascene structure 30, and the surface of the hard mask 26. A copper layer 52 is formed on the barrier layer 50.

[Para 6] The first dielectric layer 20 and the second dielectric layer 24 are dielectric materials having micro-vias, and an etching gas, like CF_4, is used to etch the first dielectric layer 20 and the second dielectric layer 24 during fabrication of the dual damascene structure 30. As a result, some of the etching gas remains in the micro-vias, preventing the barrier layer 50 from being deposited effectively on the first dielectric layer 20 and the second dielectric layer 24. As a consequence of the etching gas remaining in the micro-vias, there may be small gaps in the barrier layer 50 or the barrier layer 50 may be incompletely formed in the areas of the remaining gas. In this situation, the subsequently formed copper layer 52 effuses out through the barrier layer 50 to form the defect of copper extrusion, as indicated by numeral 70.

Summary of Invention

[Para 7] It is therefore a primary object of the claimed invention to provide a copper damascene method capable of avoiding copper extrusion.

[Para 8] According to the claimed invention, a semiconductor wafer including a substrate with at least one copper conductive wire on the substrate

is provided. A dielectric layer is formed on the copper conductive wire. Using the dielectric layer, a damascene structure having an opening to expose a portion of the copper conductive wire is formed. A degassing process is performed to make gas escape from the dielectric layer. A barrier layer overlying the surface of the exposed portion of the copper conductive wire and the damascene structure is formed. A copper layer overlying the barrier layer is formed.

[Para 9] It is an advantage that the claimed invention can avoid copper extrusion by performing a degassing process to make gas escape from the dielectric layer.

[Para 10] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[Para 11] Fig.1 shows the cross-section schematic drawing according to the dual damascene structure of the prior the art.

[Para 12] Fig.2 to Fig.4 show the damascene method schematics according to the present invention.

Detailed Description

[Para 13] Please refer to Fig.2 to Fig.4, which show damascene method schematics according to the present invention that are capable of avoiding copper extrusion. In order to make the present invention apparent, the steps

in Fig.2 to Fig.4 of the present invention similar to the prior art will use the same notations as were used in Fig.1. It is to be understood that the dual damascene process shown through Fig.2 to Fig.4 is only exemplary preferred embodiment. The present invention may be applied to single damascene processes.

[Para 14] As shown in Fig.2, a semiconductor wafer including a base layer 10 such as an interlayer dielectric with at least one copper conductive wire 14 on the base layer 10 is provided. Although not shown, the copper conductive wire 14 may electrically connect to a conductive area or device formed below the base layer 10 through a conductive plug 12. The copper conductive wire 14 may be a copper damascene layer. A first dielectric layer 20 on the copper conductive wire 14 is formed. A passivation layer 16 may be formed between the copper conductive wire 14 and the first dielectric layer 20. The passivation layer 16 may be made from silicon nitride.

[Para 15] Next, a stop layer 22, possibly made from silicon nitride, is formed overlying the first dielectric layer 20. A second dielectric layer 24 is formed on the stop layer 22. The first dielectric layer 20 and the second dielectric layer 24 are low-k dielectric layers ($k \leqq 2.9$). A hard mask 26, possibly made from silicon nitride, is formed overlying the second dielectric layer 24. A dual damascene structure 30 having an opening exposing a portion of the copper conductive wire 14 is formed in the first dielectric layer 20 and the second dielectric layer 24 using the hard mask 26 as etching mask. It is to be understood that the present invention is not limited only to a dual damascene structure but also could be applied in a single damascene structure. A tetraethoxy silane (TEOS) layer 42 may be further formed on the hard mask 26 after forming the hard mask 26.

[Para 16] Next, as shown in Fig. 3, an annealing step is performed to heat the wafer to make gas escape from the first dielectric layer 20 and the second

dielectric layer 24 as depicted by the arrows. The preferred temperature range of heating the wafer could be between 200℃ to 300℃. The annealing step could be another degassing step. The gas comprises fluorine.

[Para 17] Next, as shown in Fig. 4, a barrier layer 50 is formed on portions of the exposed surfaces of the copper conductive wire 14, the dual damascene structure 30 of the dielectric layers, and the tetraethoxy silane layer 42. Finally, a conductive layer 60 on the barrier layer 50 is formed. The conductive layer 60 could be a copper layer or another type of conductive layer. It is to be understood that application of the present invention is not limited only to preventing copper extrusion, but can also be utilized to avoid extrusion by other conductive materials.

[Para 18] Compared with the prior art, the gas remaining in the dielectric layers can escape due to a degassing step in the present invention. Therefore, the present invention can deposit the barrier layer effectively on the exposed surfaces of the dual damascene structure of the dielectric layers to avoid copper extrusion.

[Para 19] Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.